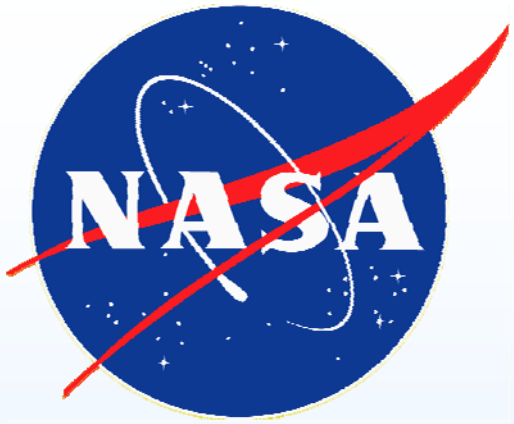

System on a Chip (SoC) Overview

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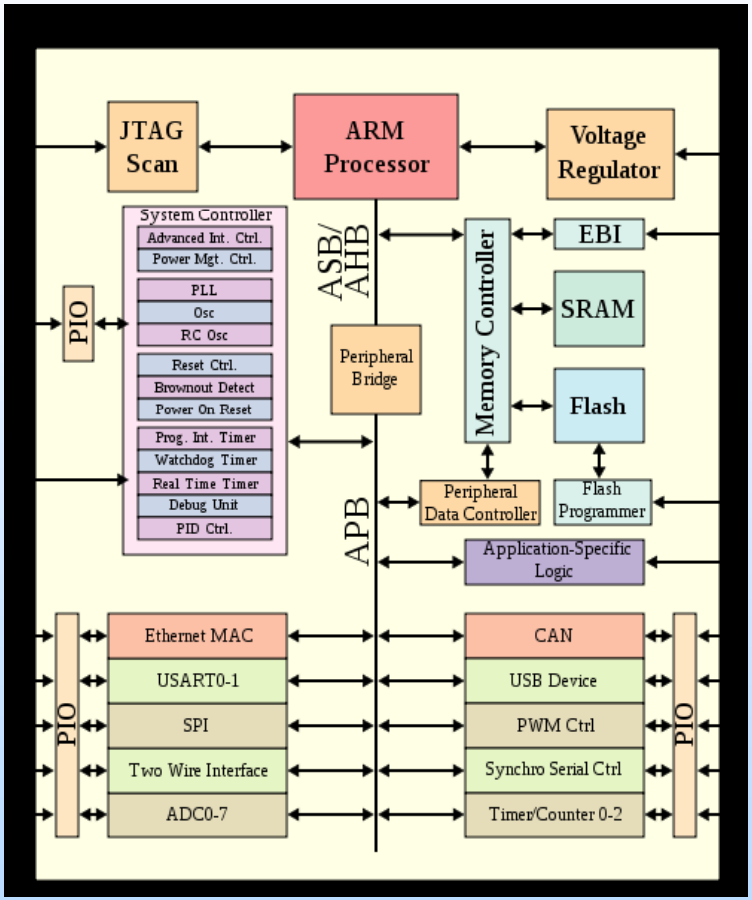
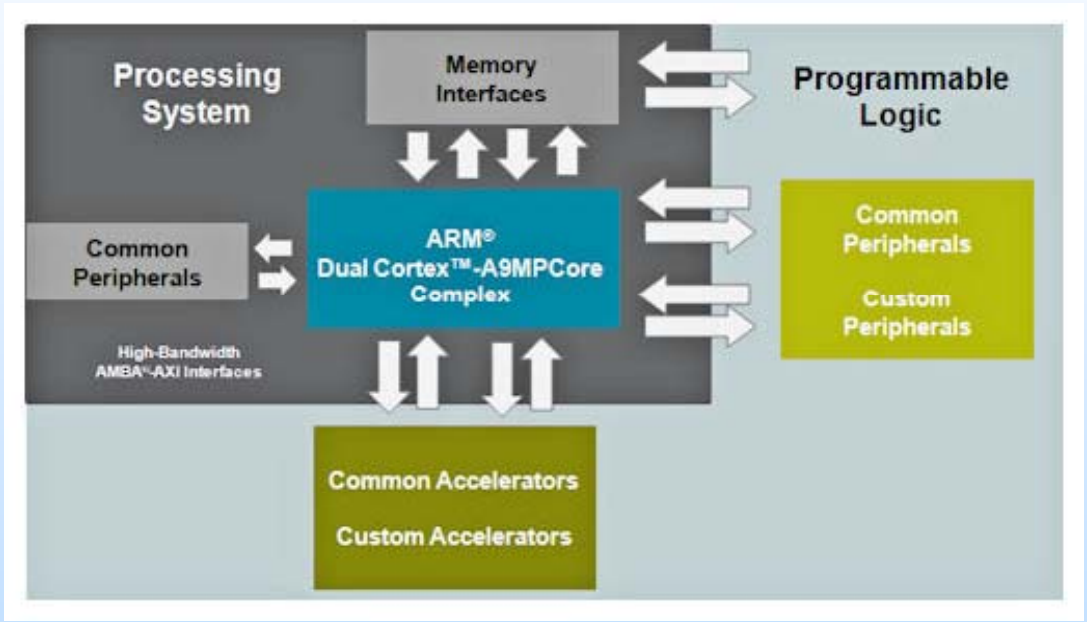
What is a SOC?

- **Wikipedia definition**
  - **System-on-a-chip or system on chip (SoC or SOC) refers to integrating all components of a computer or other electronic system into a single integrated circuit (chip). It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on a single chip substrate.**
- **A typical SoC may consist of:**
  - **One microcontroller, microprocessor or DSP core(s).**
    - **Some SoCs – called multiprocessor System-on-Chip (MPSoC) – include more than one processor core.**
  - **Memory blocks including a selection of ROM, RAM, EEPROM and flash.**
  - **Timing sources including oscillators and phase-locked loops.**
  - **Peripherals including counter-timers, real-time timers and power-on reset generators.**
  - **External interfaces including industry standards such as USB, FireWire, Ethernet, USART, SPI.**
  - **Analog interfaces including ADCs and DACs.**
  - **Voltage regulators and power management circuits.**
  - **These blocks are connected by either a proprietary or industry-standard bus such as the AMBA bus from ARM. DMA controllers route data directly between external interfaces and memory, by-passing the processor core and thereby increasing the data throughput of the SoC.**

Examples of SoCs



Standard IC version
Microcontroller-based SOC



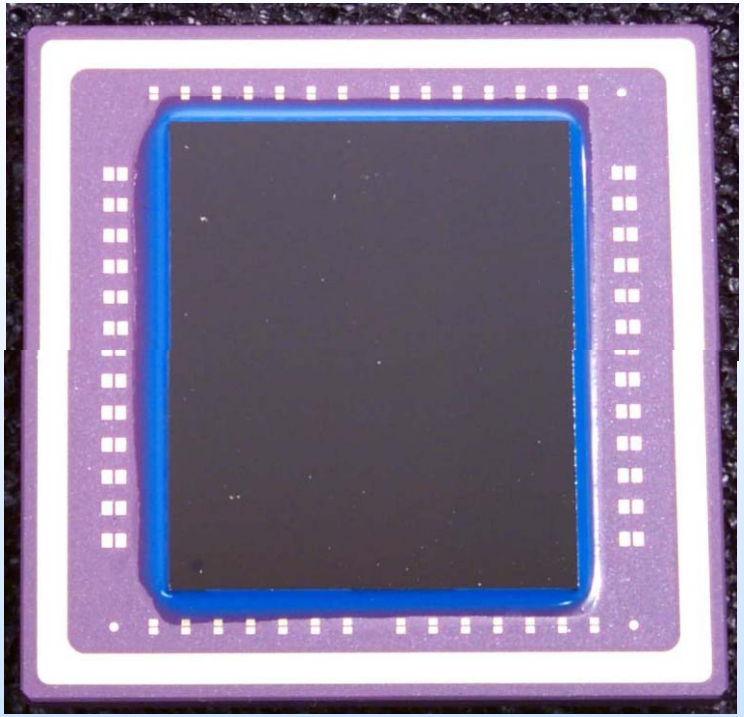
FPGA version
Microcontroller-based SOC

What types of devices are tagged SOCs?

- SoCs can be fabricated in several technologies, including:
  - Full custom
  - Standard cell
  - FPGA
- Advantages
  - Lower power and cost than the multi-chip systems that they replace.
  - Higher reliability (fewer components)
- However, like most VLSI designs, the total cost is higher for one large chip than for the same functionality distributed over several smaller chips, because of lower yields and higher NRE costs.
  - In addition, packages tend to be much larger, have a very high IO pin count, and push the state-of-the-art for new package techniques to obtain performance (non-space). Examples:
    - Upwards of 1700 pins
    - Flip-chip packages
    - Non-hermetic
    - BGA, CCGA, LGA…

Example SoC of Interest: MAESTRO Multi-Core Processor (OGA)

- **Highest Performance Rad Hard Processor**
  - 260 MHz, 38 GOPS, 19 GFLOPS
- **Tiled Architecture**
  - 49 tile, 2-D Processor Array connected by low-latency high bandwidth registermapped networks
- **Tile Processor**
  - Main Processor: 3-way VLIW CPU
    - 64-bit instruction bundle
    - 32-bit integer operations
  - Static Switch Processor
  - Floating Point Co-Processor (IEEE 754 single and double precision)
- **Memory**
  - L1 cache: 2 cycle latency
  - L2 cache: 7 cycle latency
  - Tiles can access each others L2
  - Off-chip Main Memory: 88 cycle latency
- **I/O Interfaces**
  - Four XAUI
  - Four DDR1/2
  - Two GBE



750 million transistors

18 million gates

44 million memory bits

3 million flip-flops

Largest die fabricated by IBM in 9SF (30.6X25.6 mm)

Example SoC of Interest: FPGAs

- FPGAs have been the poster child for new technologies and have replaced standard logic, ASICs, and processors in many NASA missions.
- Newer devices have even more features that make them true SoCs
  - (Re)programmable logic/fabric
  - Embedded processors/DSP strings
  - High speed IO (to 10 Gbps)
  - ADC functions, and more

"RT ProASIC®3 FPGAs are the first to offer designers of space-flight hardware a radiation-tolerant (RT), reprogrammable, nonvolatile logic integration vehicle. They are intended for low-power space applications requiring up to 350 MHz operation and up to 3 million system gates"

- **Examples of newer devices:**
  - Vilinx Virtex 4QV
    - Rad hard Virtex 5QV forthcoming
  - ACTEL RTAX4000S
    - New RTProASIC series

"Xilinx Virtex-4QV devices offer up to 200,000 logic cells, 10Mbit of RAM/FIFO, two built-in PowerPC® 405 processor blocks with an APU controller, 512 DSP™ slices, and four built-in Ethernet blocks. Virtex-4QV FPGA s deliver outstanding performance with 400Mhz clocking, DSP slices delivering 204 GMACs at 400MHz, and 350MHz PowerPC processors, all in a single device. Flexible 800 Mbps differential I/O and 500 Mbps single-ended I/O support industry-standard and custom protocols. "

Why Does NEPP Care about SOCs?

- **Potential savings of Size, Weight, and Power (SWaP) to Spacecraft as well as increased system performance**
- **Multi-core processor SoCs have sparked interest by aerospace technology developers and at multiple agencies**
  - **Example: autonomous docking operations**
- **Existing test guidance often doesn't cover new technology issues**

SoCs are pushing the state-of-the-art for both fabrication and packaging as well as design and verification/validation

Understanding qualification issues are critical to NASA mission insertion

So what's the concern?

- **Complexity drives it all**
  - **Radiation tolerance and testability are challenges for fault isolation, propagation, and validation**
  - **Bigger single silicon die than flown before and technology is scaling below 90nm (new qual methods)**
  - **Packages have changed and are bigger and more difficult to inspect, test, and understand. Add in embedded passives…**
  - **Material interfaces are more complex (underfills, processing)**
  - **New rules for board layouts. Mechanical and thermal designs, etc…**
- **How to predict radiation performance (SEU rates, etc) requires complex toolbox**
  - **DoD and NEPP are funding the tools for the toolbox**
  - **NASA OTC funding toolbox infrastructure for users – *this is at risk with NASA's recent change of technology direction***

Lesson learned:

Manufacturers are here to make money.

Believing marketing briefs is risky at best.

NEPP and SOCs

- **Efforts that follow are focused on understanding both the failure modes of this class of devices as well as developing qualification guidelines**
- **Radiation Evaluation**
  - **SoC Processors**
  - **SoC FPGAs**
  - **Predicting SEU Rates for Advanced CMOS Electronics (6/24)**
- **Parts and Package Qualification**
  - **Class Y non-hermetic qualification**
  - **Thermal reliability (hot spots!)**
  - **Design impacts**
  - **Scaled CMOS (6/24) will highlights the CMOS based issues involved**

QUESTIONS?